APPARATUS AND METHOD FOR PERFORMING STATIC TIMING ANALYSIS OF AN INTEGRATED CIRCUIT DESIGN USING DUMMY EDGE MODELING

ABSTRACT OF THE DISCLOSURE

An apparatus and method perform static timing analysis on an integrated circuit design. Certain pessimistic assumptions regarding slack when data launch and clock test signals are on opposite edges and derived from common logic blocks are improved by creating a dummy clock edge that is on the same edge as the data launch signal, and allowing the timing tool to compute the slack improvement using its native functions. The slack improvement is then multiplied by a conversion factor, and the result is used to adjust the slack. The apparatus and method give credit for slack in common blocks automatically, thereby allowing a large number of pessimistic slack values to be automatically corrected and reducing the workload of an integrated circuit designer in addressing the timing problems in an integrated circuit design.